

FIG. 1A

DIGITAL GENLOCK
BLOCK DIAGRAM

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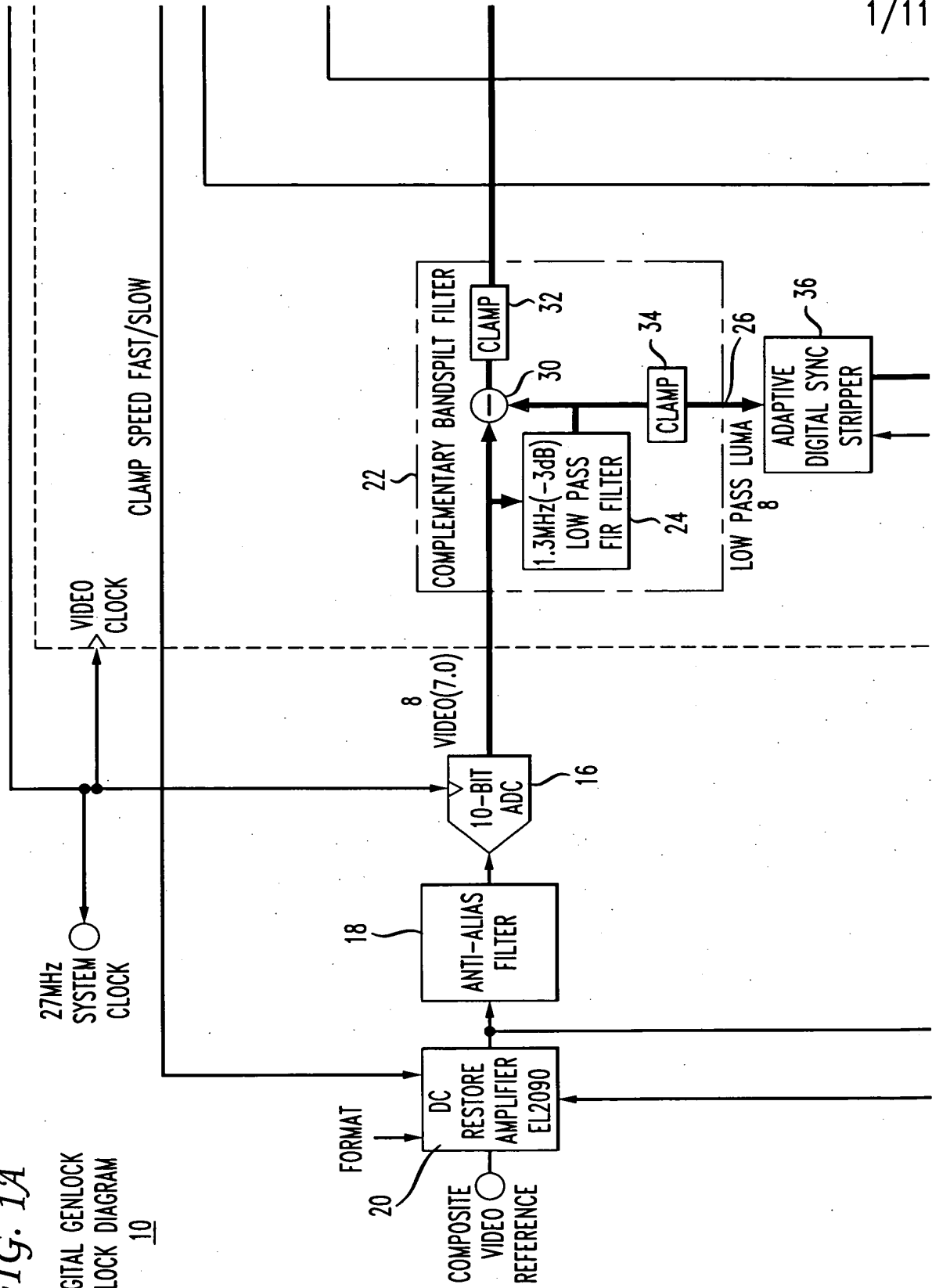
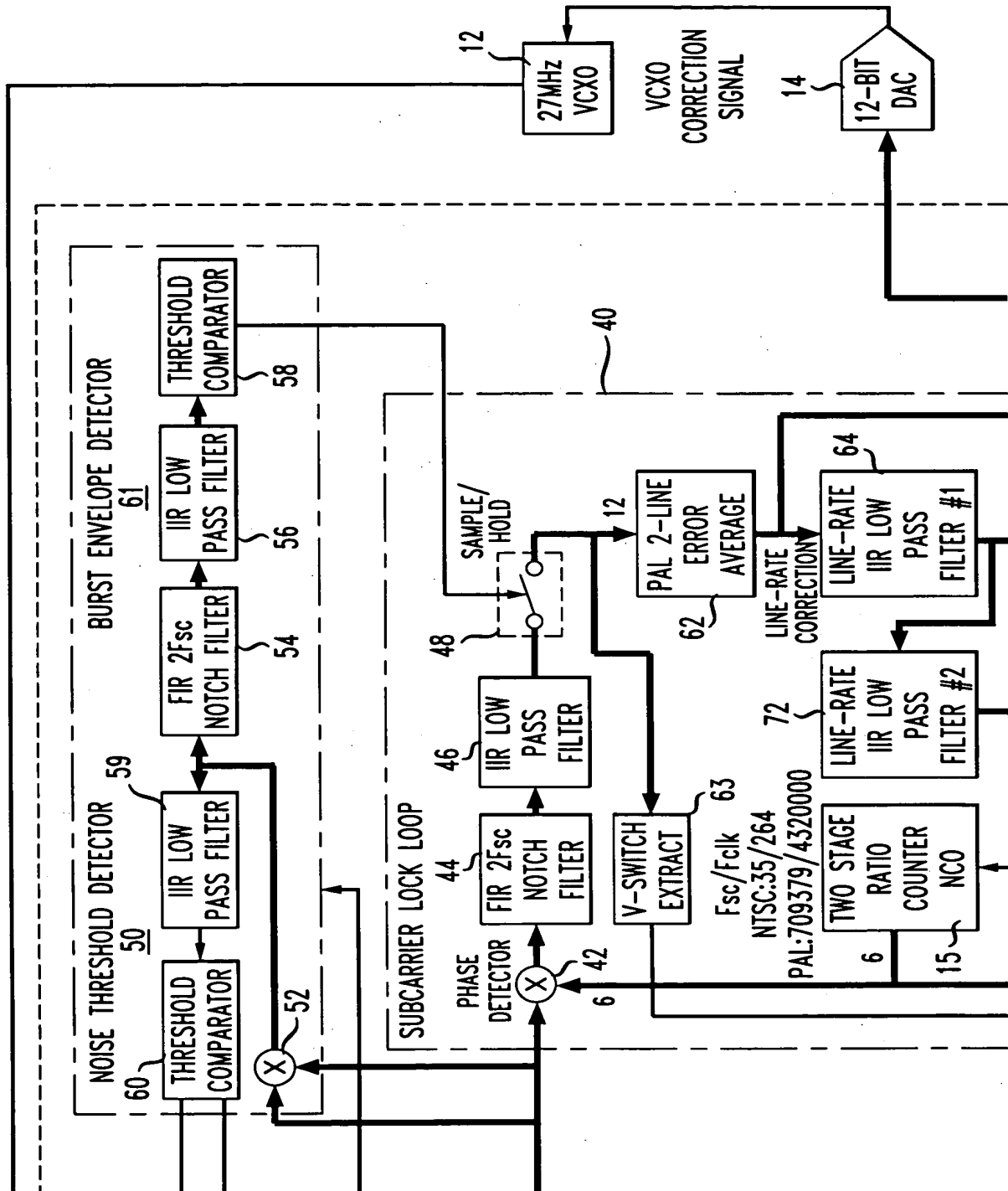


FIG. 1B

DIGITAL GENLOCK
BLOCK DIAGRAM
10

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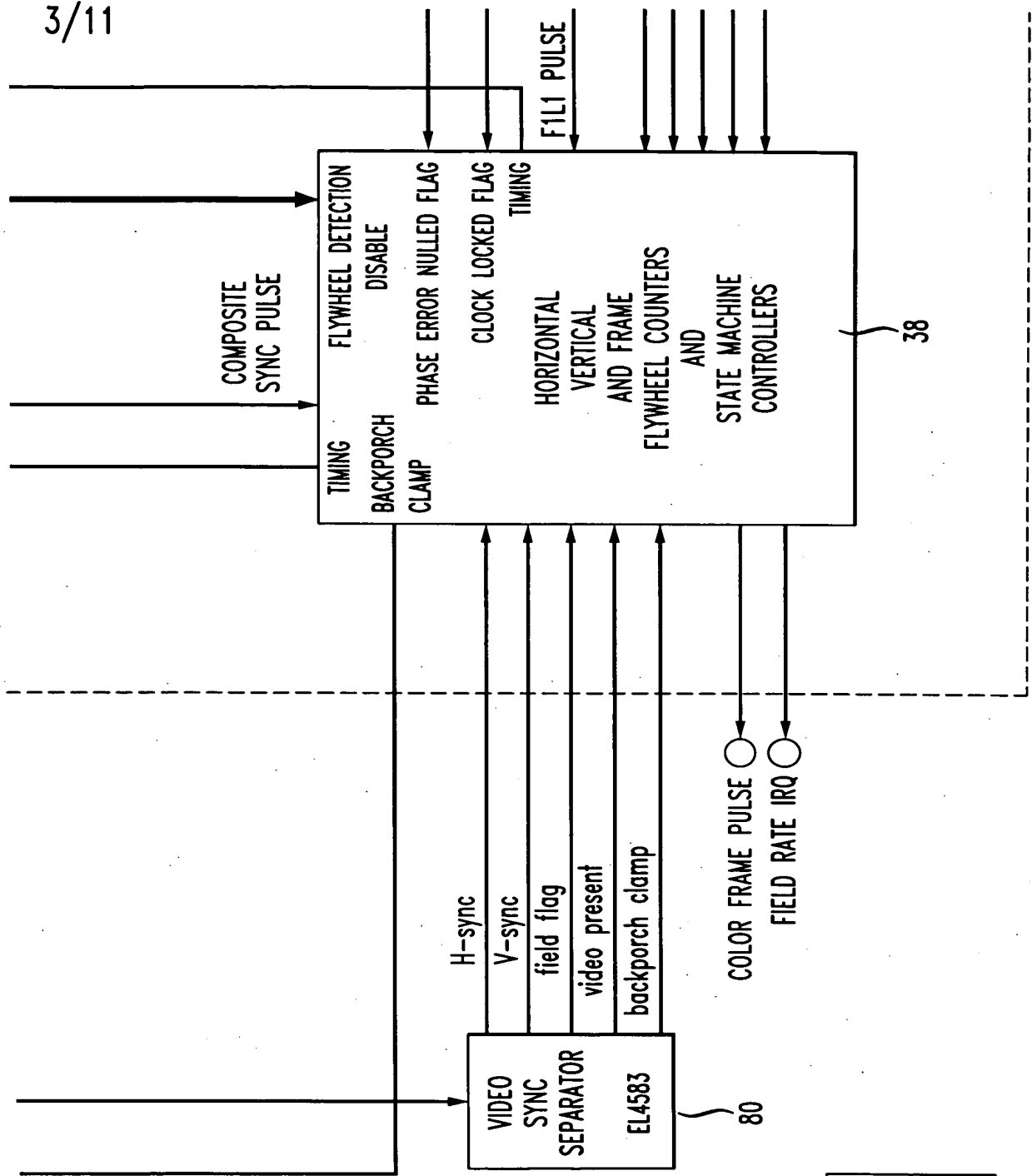


FIG. 1C
DIGITAL GENLOCK
BLOCK DIAGRAM

FIG. 1

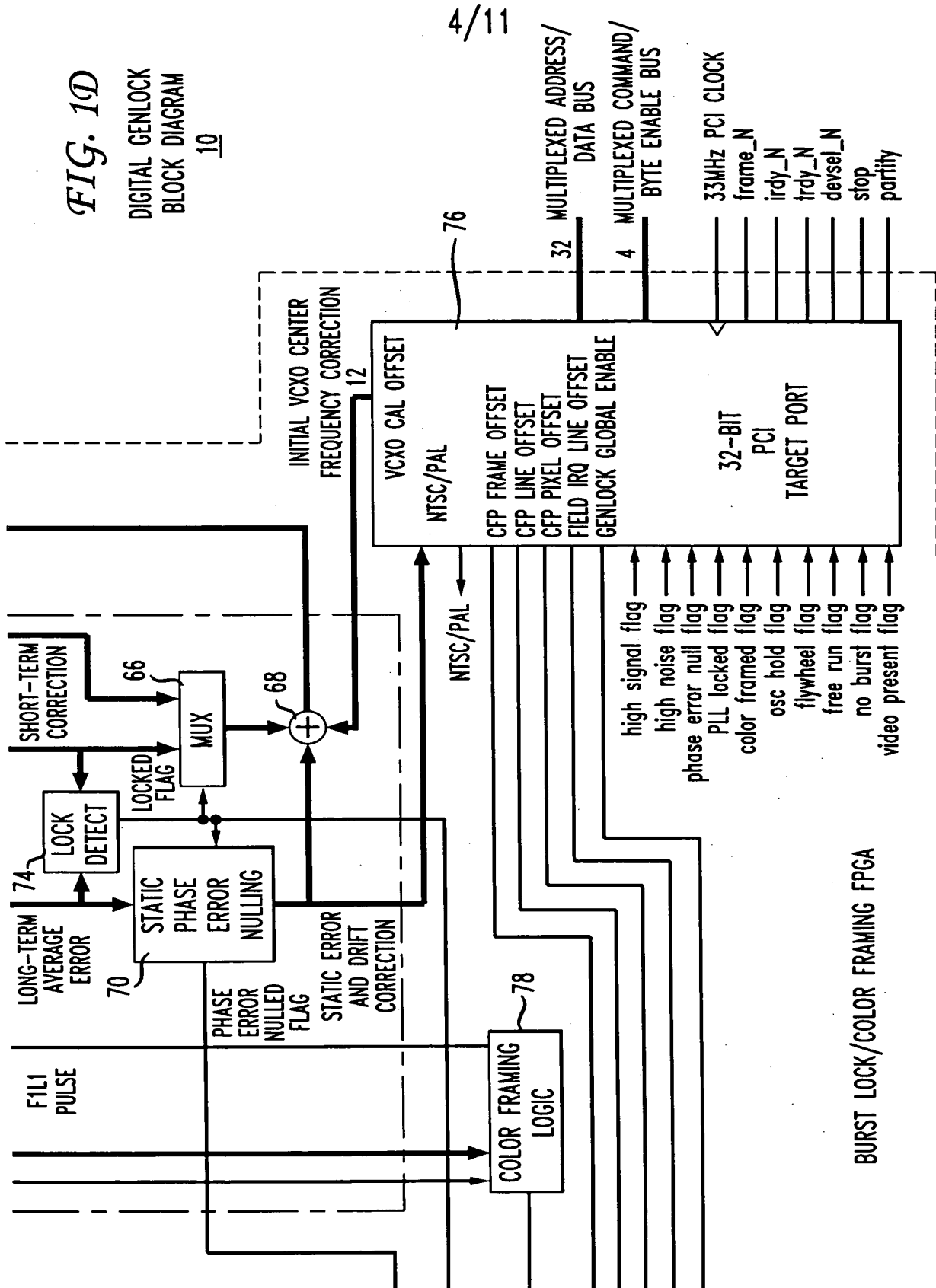
FIG. 1A	FIG. 1B
FIG. 1C	FIG. 1D

FIG. 1D

DIGITAL GENLOCK
BLOCK DIAGRAM

10

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BURST LOCK/COLOR FRAMING FPGA

FIG. 2A

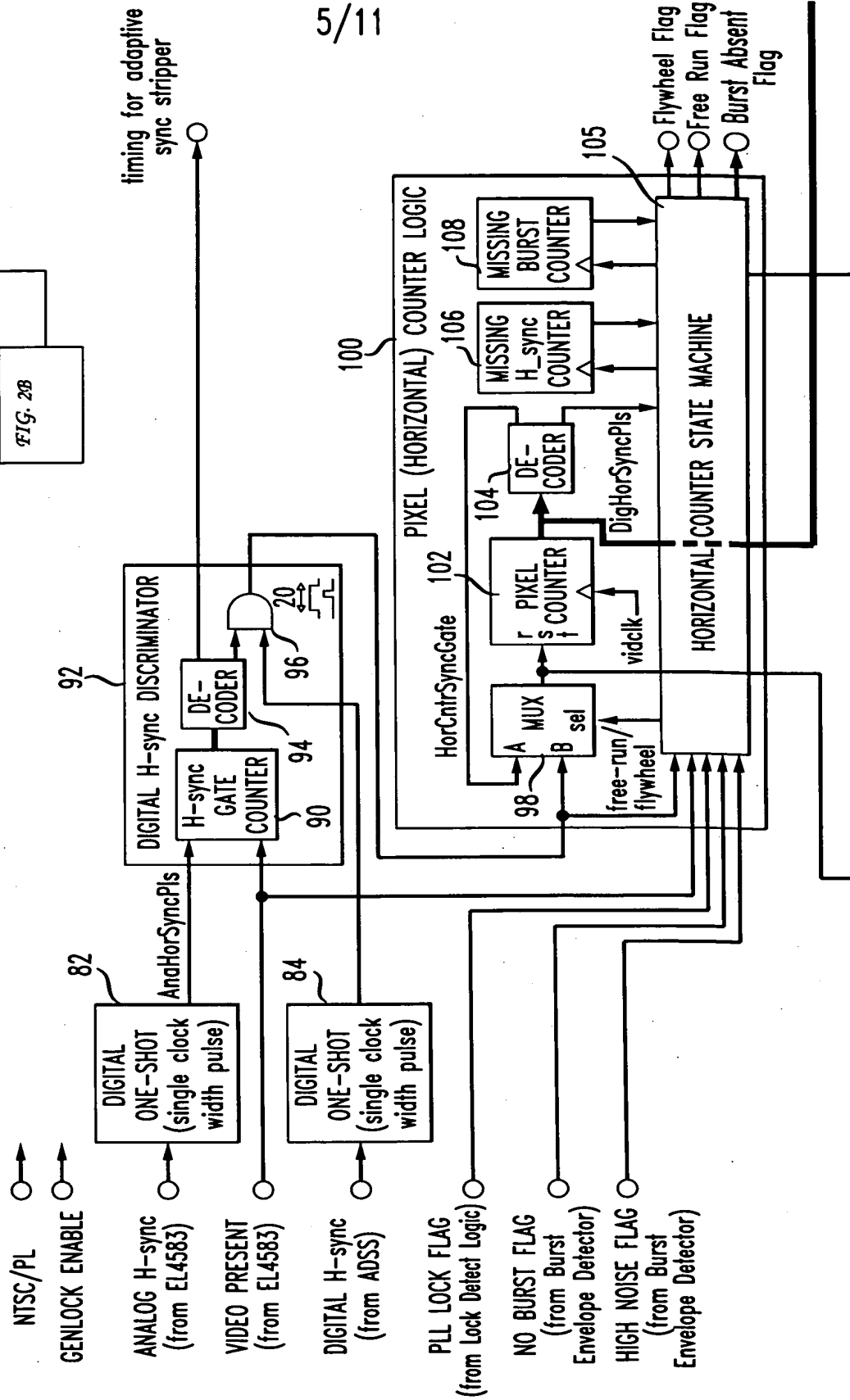


FIG. 2B

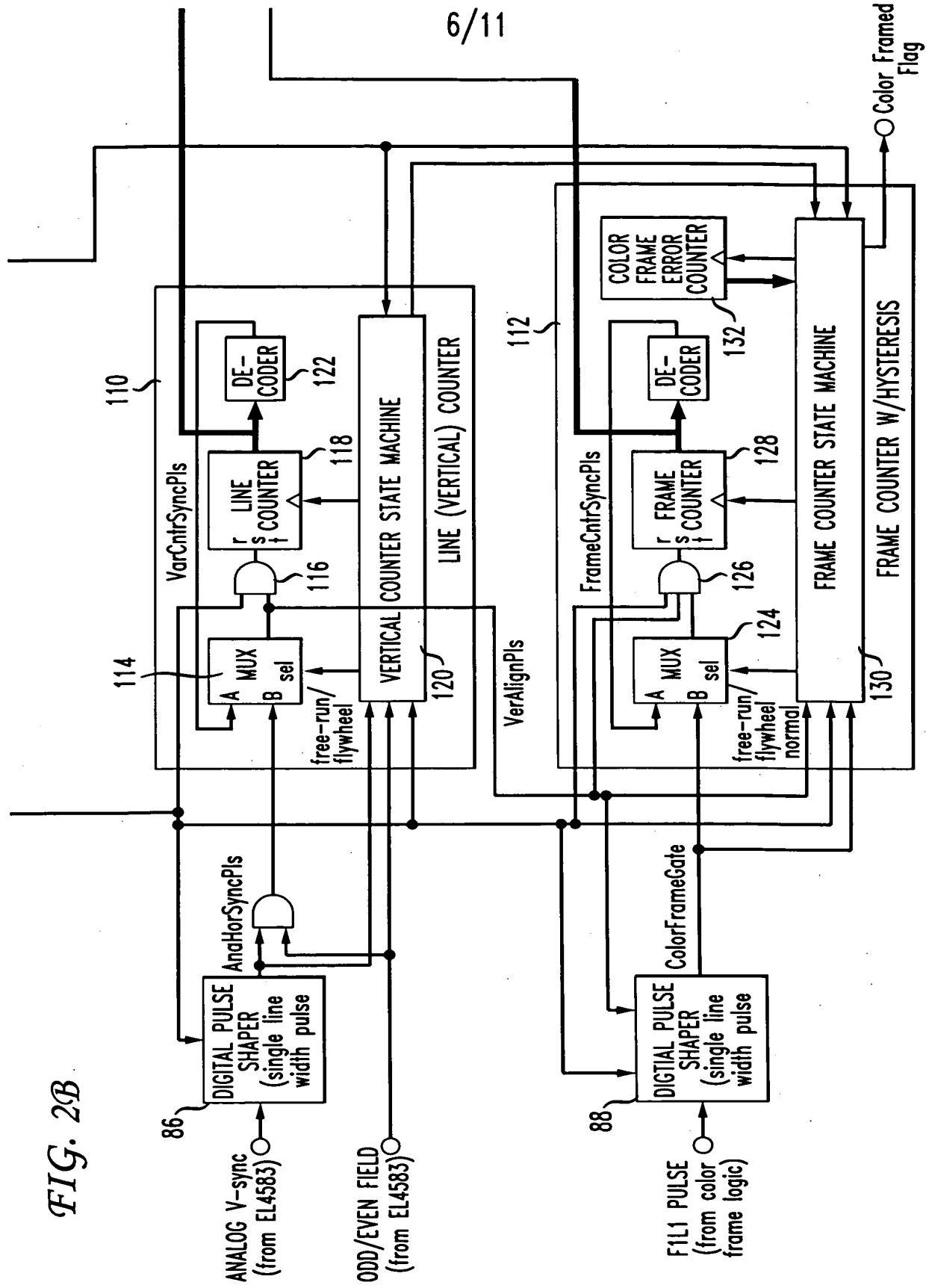


FIG. 2C

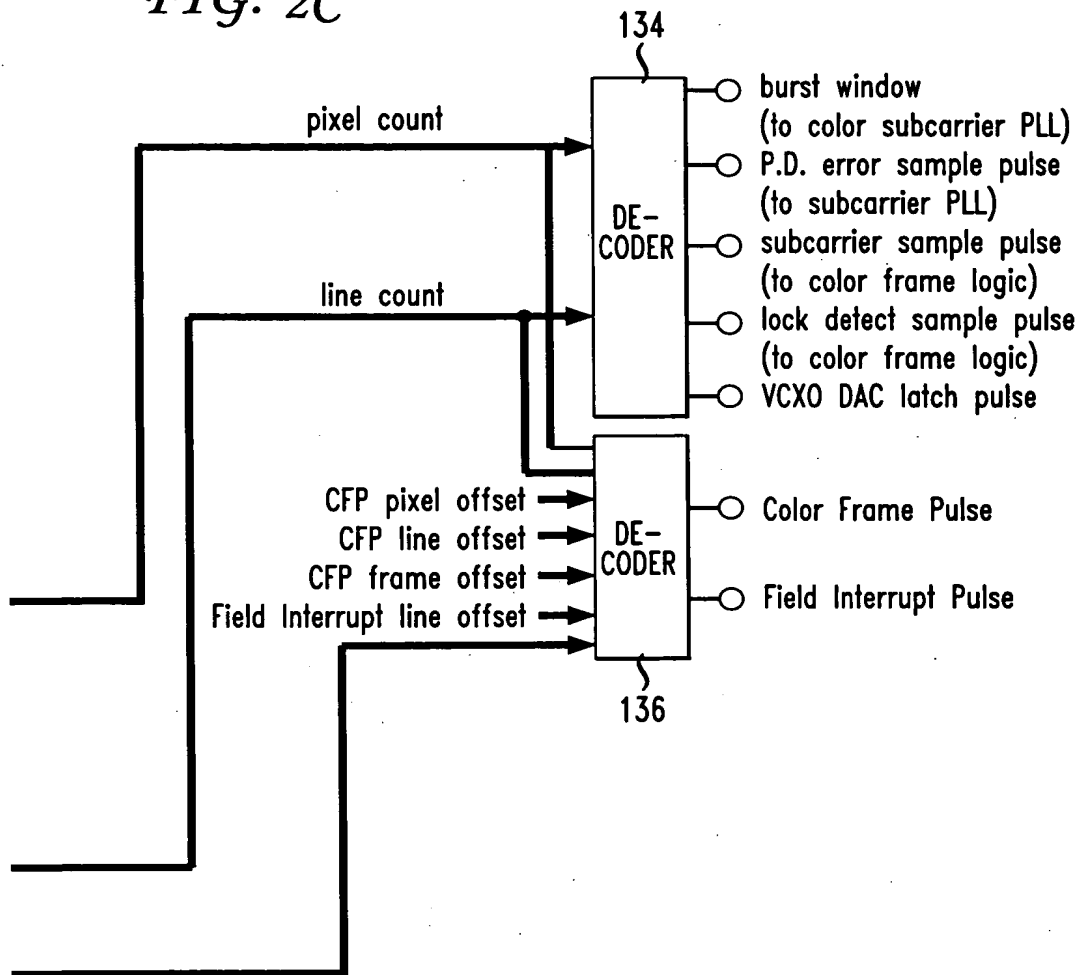


FIG. 3

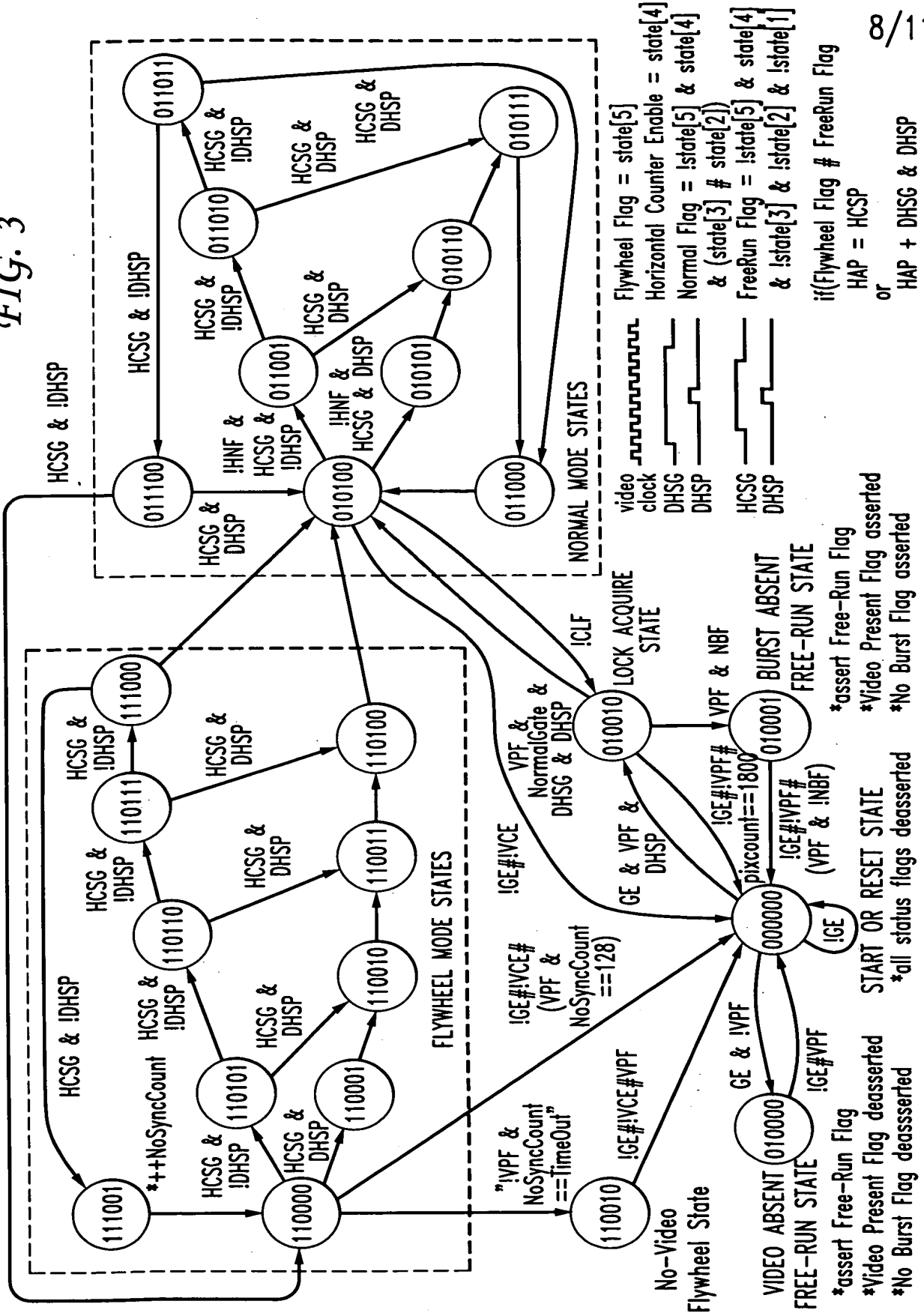
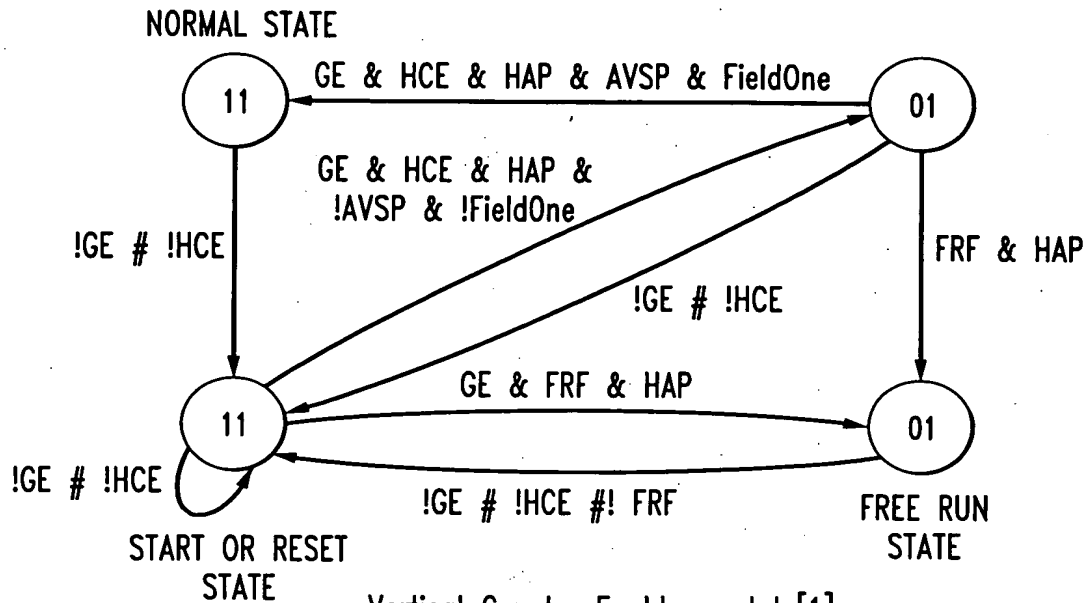


FIG. 4



Vertical Counter Enable = state[1]

if (Normal Flag # Flywheel Flag # FreeRun Flag)

VAP = VCSP

OR

VAP = AVSP & FieldOne

FIG. 5

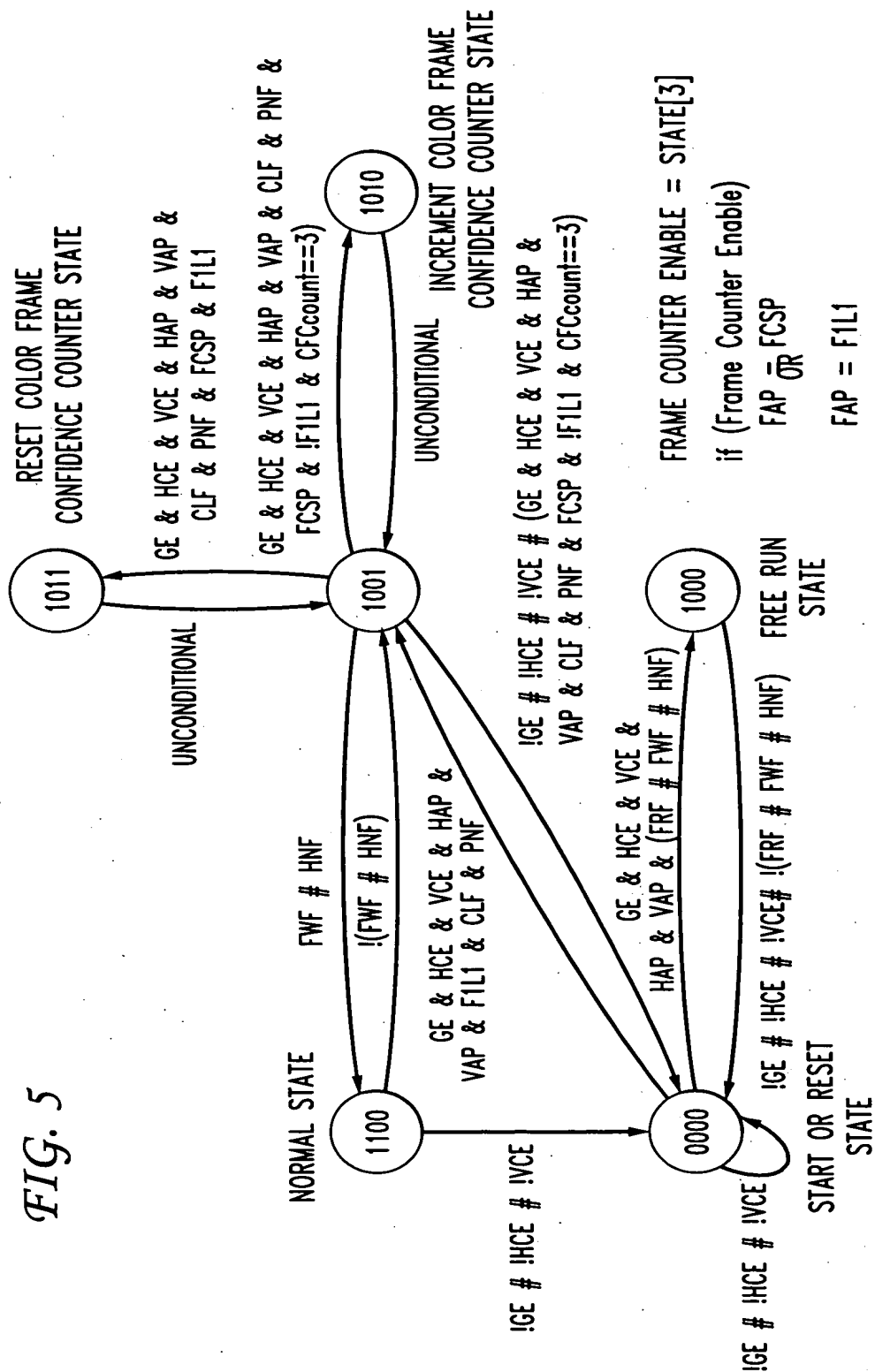


FIG. 6

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